# Chapter 1: Signals and Amplifiers

## 1.6 Frequency Response of Amplifiers

* **Amplifier bandwidth**: the range of frequencies over which the gain of the amplifier is nearly constant
  + Normally, amplifiers are designed so that their bandwidth corresponds to the frequencies of the input signals they need to amplify

|  |  |  |  |
| --- | --- | --- | --- |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |

**Bode form**: All terms are in the form

# Appendix E: Single Time Constant (STC) Circuits

* Circuits that can be reduced to one resistance (resistor) and one reactive component (inductor or capacitor)
  + Resistor and inductor:
  + Resistor and capacitor:
* Bandwidth/break/cut-off frequency

## E.1 Evaluating the Time Constant

1. Zero the voltage (short circuit)/current source (open circuit)
2. Reduce the circuit down to one resistor and one capacitor/inductor

* If multiple resistors, find the equivalent resistance seen by the capacitor/inductor
* If multiple capacitors/inductors, find the equivalent capacitance or inductance seen by the resistor
* Capacitors:
  + Series:
  + Parallel:
* Inductors:
  + Series:
  + Parallel:

## E.2 Classification of STC Circuits

|  |  |  |  |
| --- | --- | --- | --- |
| **Test at** | **Replace** | **Circuit is Low Pass if** | **Circuit is High Pass if** |
|  | C = open circuit  (since ) | Output is finite | Output is zero |
| L = short circuit  (since ) |
|  | C = short circuit  (since ) | Output is zero | Output is finite |
| L = open circuit  (since ) |

# Appendix F: s-Domain Analysis: Poles, Zeros, and Bode Plots

## F1 Poles and Zeros

For a transfer function in the form

* The **zeros** are the roots of the numerator,
  + The transfer function has zeros at
* The **poles** are the roots of the denominator, 
  + **Complex** poles/zeros always occur in conjugate pairs, i.e. if 5+3j is a zero, 5-3j is also a zero
  + **Purely imaginary** poles/zeros results in a pole/zero at

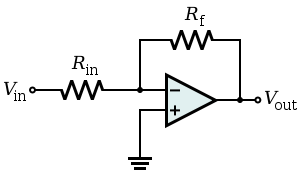
Example: has one zero at and one zero at , and poles at and

# Chapter 2: Operational Amplifiers

## 2.1 The Ideal Op Amp

* Doesn’t draw any input current: ii+ = ii- = 0
  + Input impedance of ideal op amp is infinite
  + Output impedance of ideal op amp is zero
* Infinite open-loop gain A / infinite bandwidth
  + Vi+ = Vi-(virtual short in between the terminals)

### 2.2 The Inverting Configuration



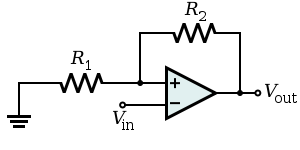
* Ideal closed loop gain:

(since for an ideal op-amp, )

* Effect of finite open-loop gain:

(since v2 is grounded, v2 = 0)

### 2.3 The Non-Inverting Configuration



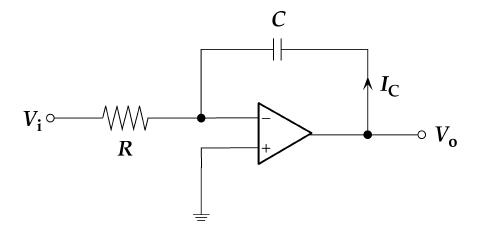
* Ideal closed loop gain:

(since for an ideal op-amp, )

* Effect of finite open-loop gain:

## 2.5 Integrators and Differentiators

### 2.5.2 The Inverting (Miller) Integrator

  
 where

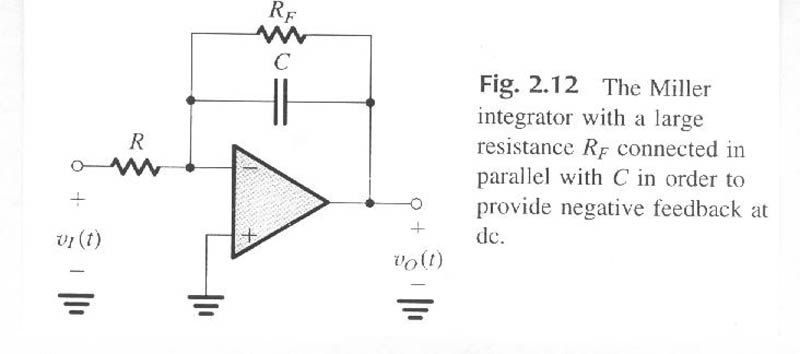
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**Transfer function:**

since , , and

and phase

To limit the DC gain, add a resistor parallel to the capacitor:

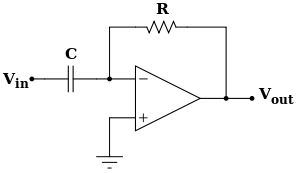


Then

Low pass filter

* As ,
* As ,
* when

### 2.5.3 The Op-Amp Differentiator



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where and

**Transfer function:**

since , , and

and phase

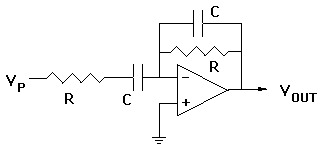
To limit the DC gain, add a resistor in series to the capacitor:

Then

High pass filter

### Band Pass Filter

Combination of integrator and differentiator



2

1

F

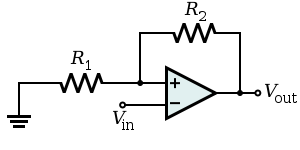
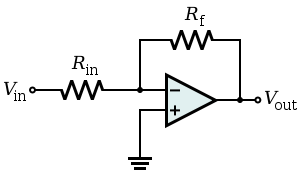
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## 2.6 DC Imperfections

### 2.6.1 Offset Voltage

* Ideally, if the two input terminals are connected together and to ground, vo = 0
* However, this isn’t the case; a finite dc voltage exists at vo
* If we connect an **input offset voltage** Vos that is same magnitude, opposite polarity as the finite dc voltage, we can balance out the op amp output vo back to 0



Vos

ground

Vos

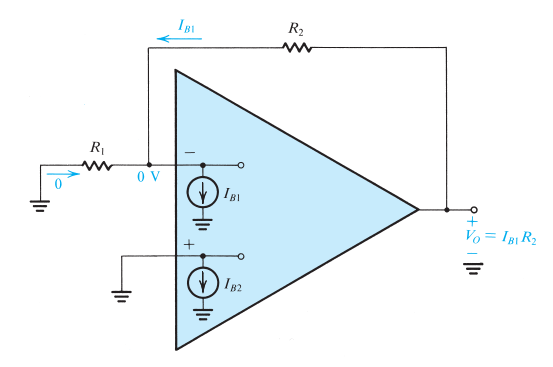
Determining the effect of Vos on the op-amp:

* Short-circuit the input voltage and add in Vos (superposition – only look at effect of Vos)
* Non-inverting and inverting configurations become the same circuit

### 2.6.2 Input Bias and Offset Currents

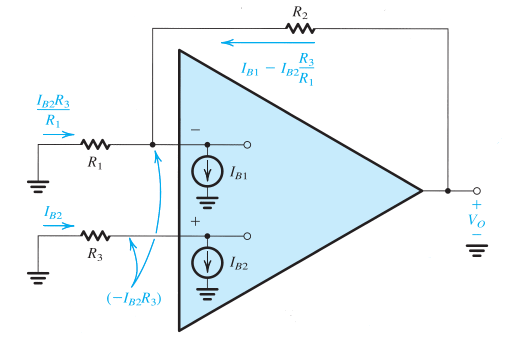
* In order for op amps to operate, they must be supplied with dc currents known as **input bias currents** IB1 and IB2
* The average value of IB1 and IB2 is the **input bias current IB:**
* The difference between IB1 and IB2 is the **input offset current IOS**:

Determining the dc offset voltage due to the input bias currents:



* Ground the input source
* Non-inverting and inverting configurations become the same circuit

Reducing the effect of IB:

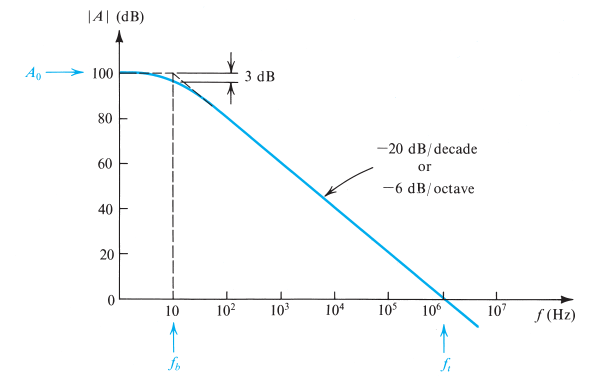


* Introduce resistance R3 in series with the non-inverting input lead (where IB2 is)
  + If IB = IB1 = IB2:
  + We can reduce Vo to zero by choosing such that , so that Vo = 0:

## 2.7 Effect of Finite Open-Loop Gain and Bandwidth on Circuit Performance

### 2.7.1 Frequency Dependence of Open-Loop Gain

* The open loop gain A of an op amp is finite – it decreases with frequency



* + – dc gain
  + – “corner/break”/3-dB frequency (frequency where gain begins to decrease)
* When :

(got rid of the 1 in the denominator) which means

* The **unity gain frequency** is the frequency when the gain reaches unity (0 dB)
  + From , and so
  + Substituting:
* The **unity gain bandwidth** is the bandwidth where the gain reaches 0 dB
  + The gain magnitude can also be expressed as:

### 2.7.2 Frequency Response of Closed-Loop Amplifiers

Inverting configuration:

Non-Inverting configuration:

## 2.8 Large-Signal Operation of Op Amps

### 2.8.1 Output Voltage Saturation

* Op amps operate linearly over a limited range of output voltages
* Op amp output saturates such that L+ and L- (upper and lower limits) are within ~1V of the positive and negative power supplies
  + E.g. an op amp with +/- 15V power supplies will saturate when the output voltage reaches around +13V in the positive direction and -13V in the negative direction, so the rated output voltage is said to be +/- 13V

### 2.8.2 Output Current Limits

* The output current of op amps is limited to a specified maximum; under no circumstances should the op amp be required to supply an output current over the maximum (in either direction)
* If the circuit requires a larger current, the op-amp output voltage will saturate at level corresponding to the maximum output current

# ECA Chapter 8: Basic RL and RC Circuits

**Resistors**

Power dissipated by a resistor:

**Inductors**

* If current is constant, V = 0
* Current can’t change instantaneously (must be continuous)

Energy stored in inductor:

**Capacitors**

* If voltage is constant, i = 0
* Voltage can’t change instantaneously (must be continuous)

Energy stored in capacitor:

## 8.1 The Source-Free RL Circuit – Natural Response

**Natural response**: a circuit’s response to stored energy

## 8.2 Properties of the Exponential Response

**Time Constant**

𝜏 = the time it takes to decrease from unity to 0, assuming a constant rate of decay

* For RL circuits,
* For RC circuits,

## 8.3 The Source-Free RC Circuit – Natural Response

## 8.4 A More General Perspective

* For inductors,
* For capacitors,

## 8.6–8.8 Step Response of RC/RL Circuits

**First order circuit**: A circuit that can be reduced to one with a single energy storage element (inductor or capacitor)

**Step response**: A circuit’s response to a step (abrupt) change in its input

1. Find the initial and final values of the variable of interest –
2. The solution is equal to
3. or

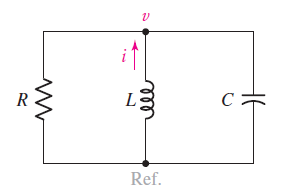
# Chapter 9: The RLC Circuit

## 9.1 The Natural (Source-Free) Response of Parallel RLC Circuits

**Resistor:**

**Inductor:**

**Capacitor:**



KCL at node:

Differentiate to get a 2nd order differential equation:

Assume that the solution is in the form:

Substitute into differential equation:

Solve:

Define:

**Neper Frequency:**

**Resonant Frequency:**

### Case 1: Two real roots () – Overdamped

### Case 2: Repeated real roots () – Critically damped

### Case 3: Complex roots () – Underdamped

**Natural Resonant Frequency**

### Solving a Parallel RLC Circuit

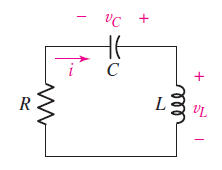
1. Determine damping (compare to )
2. Select correct form of equation
3. Use two initial conditions and to solve for constants

## 9.5 The Natural (Source-Free) Series RLC Circuit

**Resistor:**

**Inductor:**

**Capacitor:**



KVL around loop:

Differentiate for 2nd order differential equation:

Assume that the solution is in the form:

Substitute into equation:

Solve:

Define:

**Neper Frequency:**

**Resonant Frequency:**

### Solving a Series RLC Circuit

1. Determine damping (compare to )
2. Select correct form of equation
3. Use two initial conditions and to solve for constants

## 9.6 The Complete Response of the RLC Circuit

Complete response = natural response + forced response

Parallel circuits:

Series circuits:

### Solving for the Complete Response

1. Determine initial conditions and
2. Obtain numerical value for forced response
3. Complete response = appropriate form of the natural response + forced response
4. Evaluate the response and its derivative at t=0 and use initial conditions to solve for constants

# Chapter 3/4: Diodes

## Non-Linear Circuits

Linear Circuits

* If a source changes by a factor *k*, all currents and voltages also change by *k*
* Obeys superposition, i.e.
* If input is a sine wave, output is at **same frequency** (amplitude/phase might change)

Non-Linear Circuits

* Recall:
* Doesn’t always obey superposition, i.e.

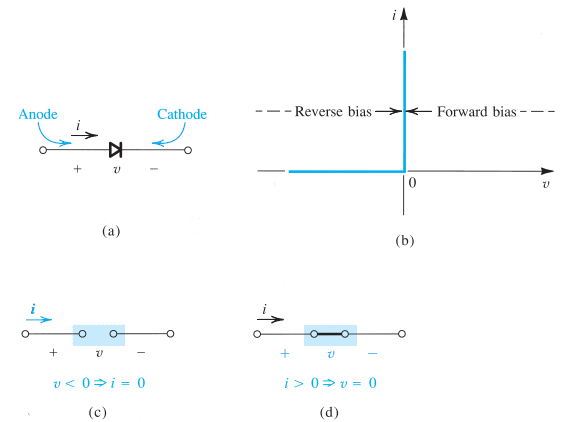
Example:

If:

If:

* DC bias
* Signal multiplied by gain (10 in the above equation)
* Distortion - ~1% of the signal (very small)

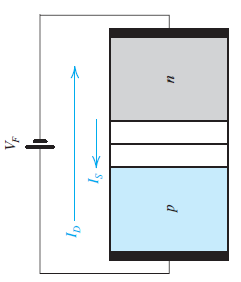
## 4.1 The Ideal Diode



* – diffusion current
* – drift current
* **Reverse bias**: – diode is off, behaves like **open circuit**
* **Forward bias**: – diode is on, behaves like a **short circuit**

## 4.2 Real Diode Behaviour

### Forward Bias



* + Depletion region narrows, so electric potential decreases
  + increases – net positive
  + remains constant

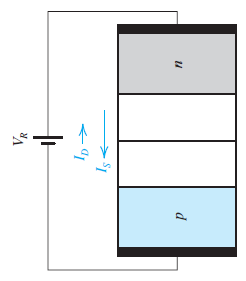
Terminal voltage

* is the saturation current/**scale current** and is constant for a given diode at a given temperature
* is the **thermal voltage**, ~25 mV at room temperature (20°C)
* We can approximate
* Hence,

Given two sets of :

A 1mA diode has when

### Reverse Bias



* + Depletion region widens, so electric potential increases
  + decreases – net negative
  + remains constant
  + We can approximate

## 4.3 Modeling the Diode Forward Characteristic

### 4.3.1 The Exponential Model

To find vD and iD:

1. Determine if the diode is on or off
2. Estimate iD from the circuit
3. Use iterations of iD and to find iD and vD

### 4.3.5 The Constant-Voltage-Drop Model

Diode off:

Diode on:

### 4.3.6 The Ideal Diode Model

Diode off:

Diode on:

**Choosing the right model:**

* When voltages in the circuit >> vD, simple models are suitable
* If we need vD, must use exponential model

### 4.3.7 The Small-Signal Model

A diode with a DC voltage and a small AC voitage

VD = DC voltage, vd(t) = AC voltage

Then:

Since :

If the amplitude of the AC signal is kept sufficiently small, i.e. :

Then we can see that , where – id is directly proportional to vd

**The Diode’s Small Signal Resistance**

From

**A Linearized Model of the Diode**

1. Set the small signal (AC) to 0 and analyze the DC circuit using a diode model (CVD)
2. Replace the diode with its linearized model vD, ID, and rd

* Note: since DC sources get zeroed anyway in the next step, can just replace diode with rd

1. We now have a linear circuit, so set all DC sources to zero and find the output due to the small signal vd(t)
2. Add the DC value (step 1) to the AC value (step 3) to get the total output

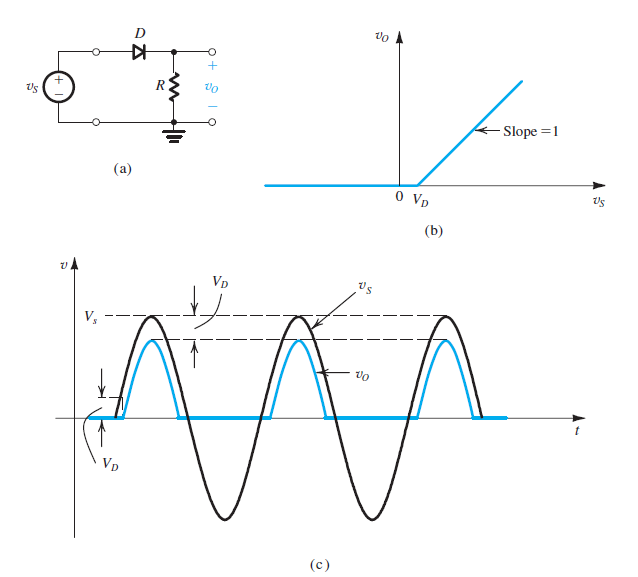
## 4.6 Diode Rectifiers

Rectifiers allow us to obtain a DC voltage from an AC voltage

### 4.5.1 The Half-Wave Rectifier

If , then

If , then

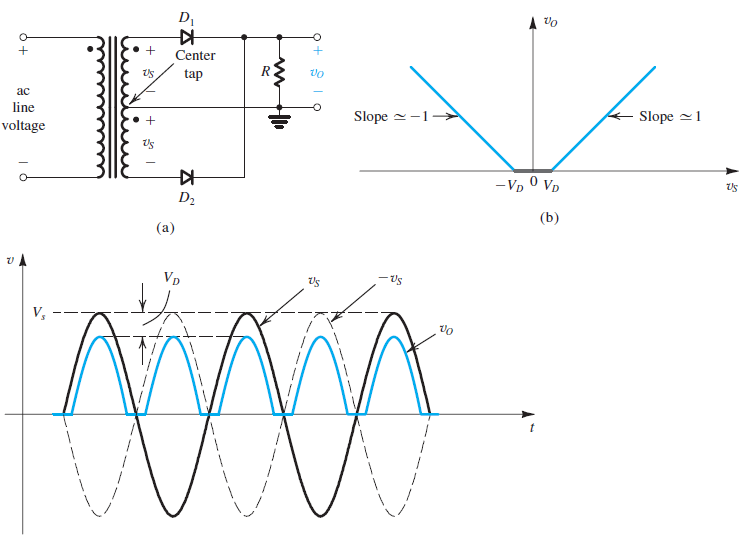


* **Peak Inverse Voltage:** maximum voltagethat diode can withstand before breakdown
* (peak of Vs)
* for ideal diodes ( for CVD model)

### 4.5.2 The Full-Wave Rectifier

When , D1 is on and so D2 must be off

When , D2 is on and so D1 must be off



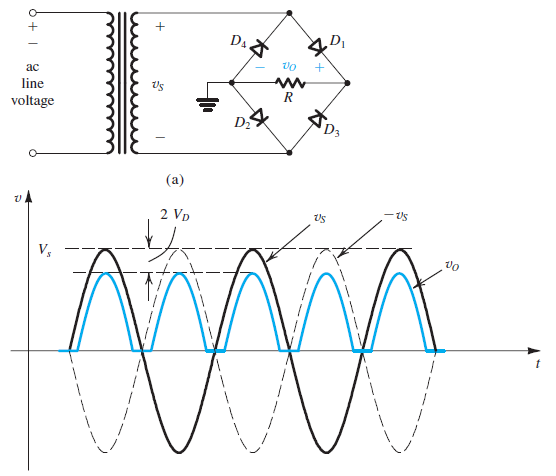


### 4.5.3 The Diode Bridge Rectifier

When , D1 and D2 are on (forward bias) while D3 and D4 are off (reverse bias)

When , vice versa

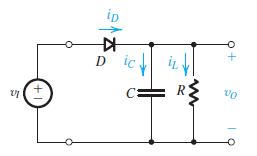
* Since there are two diodes at a time in conduction path,

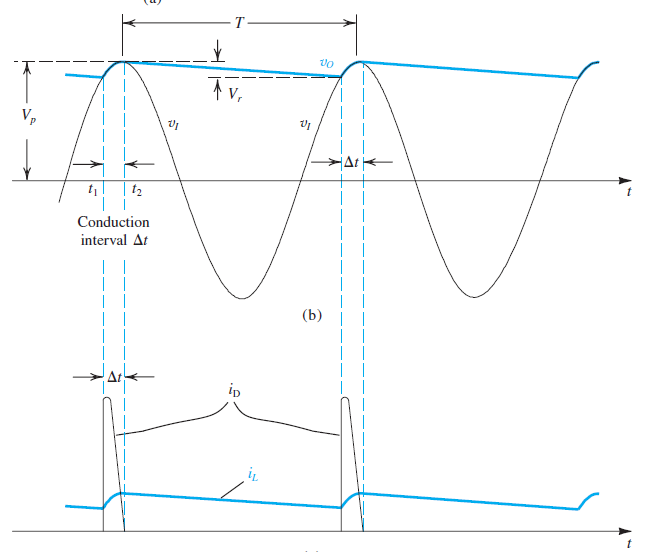


### 4.5.4 The Rectifier with a Filter Capacitor – The Peak Rectifier

A **filter capacitor** can be added across the load resistor, to smooth out the output voltage – the circuit outputs the peak of the input sine wave

* Capacitor C charges to the peak of the input ()
* Diode turns off and C discharges through resistor R
* When exceeds the capacitor voltage, the diode turns on again and charges the capacitor up to





* is the time interval where the diode is on
* is approximately the discharge interval of the capacitor
  + During this time, C discharges through R, so decays exponentially with time constant –
* At the end of the discharge interval, , where is the **ripple voltage** – we assume it is much smaller than
* When is very small, is nearly constant the peak input voltage, so the DC output voltage ; then we can say

When the diode is off (during the discharge interval):

At the end of the discharge interval:

To keep small, we make . Then we can approximate :

**To find :**

Approximate :

**To find average diode current during conduction**:

Charge that diode supplies to C = charge that C loses during discharge interval

**The maximum capacitor charging current:**

## Summary

### Half-wave rectifier with a capacitor

### Full-wave rectifier with a capacitor

Ripple voltage is cut in half: